

IN THE CLAIMS:

Claims 5 and 12-24 were previously cancelled. Claims 1-4 and 6-11 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently amended) A method of fabricating a multi-level stack of semiconductor substrate elements, each semiconductor substrate element of ~~said~~ the substrate elements including integrated circuitry, comprising:
providing a first semiconductor substrate element having a first side including integrated circuitry thereon and having a back side in a first wafer having a periphery having a portion thereof including a flat;
providing a second semiconductor substrate element having a first side including integrated circuitry thereon and having a ~~backside~~ back side in a second wafer having a periphery having a portion thereof including a flat;
providing a heat sink element for ~~said~~ the multi-level stack between the first and second semiconductor substrate elements;
stacking ~~said~~ the first semiconductor substrate element and the second semiconductor substrate element in a superimposed relationship having the back side of the first semiconductor substrate element facing the back side of the second semiconductor substrate element having the periphery of ~~said~~ the first semiconductor substrate element substantially aligned with the periphery of ~~said~~ the second semiconductor substrate element, ~~said~~ the first semiconductor substrate element and the second semiconductor substrate element for locating a portion of the integrated circuitry on ~~said~~ the first semiconductor substrate element vertically spaced from a portion of the integrated circuitry on the second semiconductor substrate element for vertical alignment of ~~said~~ the first semiconductor substrate element and ~~said~~ the second semiconductor substrate element; and

severing from ~~said the multi-stack~~ stack transversely at least one dice pair comprising a die from ~~said the~~ first semiconductor substrate element and a second die from ~~said the~~ second semiconductor substrate element; and adhesively attaching ~~said the~~ first semiconductor substrate element and ~~said the~~ second semiconductor substrate element.

2. (Currently amended) The method of claim 1, wherein ~~said adhesive~~ adhesively attaching comprises a dielectric adhesive.

3. (Currently amended) The method of claim 1, further including: disposing the heat sink element between ~~said the~~ first semiconductor substrate element and ~~said the~~ second semiconductor substrate element.

4. (Currently amended) The method of claim 1, wherein ~~said first semiconductor substrate element and the second semiconductor substrate element~~, each semiconductor substrate element of the first semiconductor substrate element and the second semiconductor substrate element including locations defining discrete dice or wafer portions severable from a first semiconductor substrate wafer and at least one second substrate wafer.

5. (Cancelled)

6. (Currently amended) The method of claim 1, further comprising: connecting a first die of ~~said the~~ at least one dice pair to a substrate having conductors.

7. (Currently amended) The method of claim 6, wherein ~~said connection is~~ connecting includes a connection selected from a group comprising reflowable metal elements, polymer elements having a conductive capability, and preformed lead-type elements.

8. (Currently amended) The method of claim 6, further comprising:
connecting both dice of ~~said~~ the at least one dice pair to ~~said~~ the conductors of ~~said~~ the
substrate.

9. (Currently amended) The method of claim 1, further comprising:
connecting ~~the~~ a second die of ~~said~~ the at least one dice pair to conductors of ~~said~~ the substrate
through intermediate connection elements.

10. (Currently amended) The method of claim 9, wherein ~~said~~ the intermediate
connection elements are selected from a group consisting of bond wires and traces of flex
circuits.

11. (Currently amended) The method of claim 10, further comprising:
connecting ~~said~~ the at least one dice pair to portions of the conductors of ~~said~~ the substrate and
encapsulating ~~said~~ the at least one dice pair thereafter.

12.-24. (Cancelled)